REMARKS

Claims 3-10 and 21-35 are pending in the present application.

Drawings

Applicant notes the Examiner's acceptance of the corrected drawings as filed along with the Amendment dated August 29, 2005

Claim Rejections-35 U.S.C. 103

Claims 3-10 and 21-35 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Itonaga reference (U.S. Patent Application Publication No. 2002/0061639) in view of the Yu et al. reference (U.S. Patent Application Publication No. 2003/0029715). The Examiner has relied upon somewhat similar reasons as in the previous Office Action dated May 18, 2005. This rejection is respectfully traversed for the following reasons.

The method for fabricating a semiconductor device of claim 21 includes in combination "forming a metallic silicide layer in an interface between the silicon region and the metallic layer under the protective layer by a first heat treatment, so that the metallic silicide layer has a high resistance crystalline structure"; "removing the protective layer"; and "subjecting the metallic silicide layer to second heat treatment after said removing the protective layer, so that the metallic silicide layer has a low resistance crystalline structure". Applicant respectfully submits that the prior art as

relied upon by the Examiner does not make obvious these features.

As emphasized in the Remarks section on page 11 of the Amendment dated August 29, 2005, as described in paragraph [0071] of the Itonaga reference with respect to Fig. 1C, formation of a metallic silicide layer 10a under protective layer 9 between silicon layer 7 and metal layer 8 is by a first rapid thermal anneal (RTA). The protective layer 9 and the unreacted metal film 8a are then removed, as described in paragraph [0073] and as shown in Fig. 2A. Thereafter, arsenic ions are implanted into metal silicide film 10a "so as to turn the polysilicon or silicon into an amorphous state", as described in paragraph [0074] with respect to Fig. 2B. As described in paragraph [0076] of the Itonaga reference with respect to Fig. 2C, the structure is then subjected to a second RTA so as to convert the amorphous metal silicide film 10b into a structurally-stable silicide layer 10c.

Accordingly, the Itonaga reference as relied upon by the Examiner discloses the following in sequential order: (1) formation of metallic silicide layer 10a in a first RTA; (2) removal of protective layer 9 and unreacted metal film 8a; (3) implantation of arsenic ions into metal silicide film 10a so as to form amorphous metal silicide film 10b; and (4) a second RTA to convert amorphous metal silicide film 10b into a structurally-stable polycrystalline metal silicide film 10c.

That is, the second RTA as described in paragraph [0076] of the Itonaga reference with respect to Fig. 2C, converts **amorphous** metal silicide film 10b into polycrystalline metal silicide film 10c. The second RTA as described in paragraph

[0076] of the Itonaga reference does not convert a metallic silicide layer having a high resistance crystalline structure into a metallic silicide layer having a low resistance crystalline structure, as would be necessary to meet the features of claim 21. This should be especially clear because first metal silicide film 10a is converted into an amorphous metal silicide film 10b as described in paragraph [0074] with respect to Fig. 2B, **prior to** the second RTA.

In the Response to Argument Section on page 8 of the Final Office Action, the Examiner has asserted that "whether or not Itonaga teaches forming an amorphous layer as an intermediate step is irrevelant in so far as there is no language in Applicant's claims that precludes an amorphous layer from being formed as an intermediate step".

Applicant respectfully submits that the Examiner has failed to appreciate the scope of claim 21 as pending. As noted above, the second heat treatment of claim 21 changes a metallic silicide layer **having a high resistance crystalline structure** into a metallic silicide layer having a low resistance crystalline structure. In view of this, the metallic silicide layer has a crystalline structure even during an intermediate stage of the process. Regardless of the Examiner's assertion that claim 21 may not include language that precludes an intermediate step (which Applicant does not necessarily agree), the second RTA as described with respect to Fig. 2C of the Itonaga reference converts an **amorphous** metal silicide layer into a polycrystalline metal silicide layer. The second RTA as described with respect to Fig. 2C of the Itonaga reference does not

convert a metallic silicide layer having high resistance crystalline structure into a metallic silicide layer having low resistance crystalline structure, as would be necessary to meet the features of claim 21. The Itonaga reference as relied upon by the Examiner thus fails to meet the features of claim 21. The Examiner has failed to establish any motivation for modifying the process of the Itonaga reference so as to meet these particular features of claim 21. Also, the secondarily relied upon Yu et al. reference does not overcome the above noted deficiencies of the Itonaga reference. Applicant therefore respectfully submits that the method for fabricating a semiconductor device of claim 21 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 3-10, 21 and 22 is improper for at least these reasons.

The method of manufacturing a semiconductor device of claim 23 includes in combination subjecting a first metallic silicide layer having a high resistance crystalline structure to a second heat treatment so as to change the first metallic silicide layer into a second metallic silicide layer having a low resistance crystalline structure.

As asserted previously with respect to claim 21, during the second RTA as described in paragraph [0076] with respect to Fig. 2C of the Itonaga reference, an **amorphous** metal silicide film 10b is converted into a polycrystalline metal silicide film 10c. The Itonaga reference as relied upon by the Examiner does not specifically disclose a second heat treatment that changes a first metallic silicide layer having a high resistance crystalline structure into a second metallic silicide layer having a low

resistance crystalline structure. Applicant therefore respectfully submits that the method of manufacturing a semiconductor device of claim 23 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 23-29 is improper for at least these reasons.

The method of manufacturing a semiconductor device of claim 30 includes in combination subjecting a high resistance metallic silicide layer having a first crystalline structure to a second heat treatment so as to change the high resistance metallic silicide layer into a low resistance metallic silicide layer having a second crystalline structure.

As noted above, the Itonaga reference as relied upon by the Examiner includes a second RTA that converts an **amorphous** metal silicide layer into a polycrystalline metal silicide layer. The Itonaga reference as relied upon by the Examiner does not specifically disclose a second heat treatment that changes a high resistance metallic silicide layer having a first crystalline structure into a low resistance metallic silicide layer having a second crystalline structure, as would be necessary to meet the features of claim 30. Applicant therefore respectfully submits that the method of manufacturing a semiconductor device of claim 30 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 30-35 is improper for at least these reasons.

Conclusion

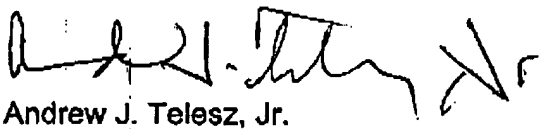
The Examiner is respectfully requested to reconsider and withdraw the corresponding rejection, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



Andrew J. Telesz, Jr.
Registration No. 33,581

One Freedom Square
11951 Freedom Drive, Suite 1260
Reston, Virginia 20190
Telephone No.: (571) 283-0720
Facsimile No.: (571) 283-0740